Design of a Readout System for Testing the Electronics of the CMS Experiment Barrel Muon Trigger at the HL-LHC Accelerator at CERN

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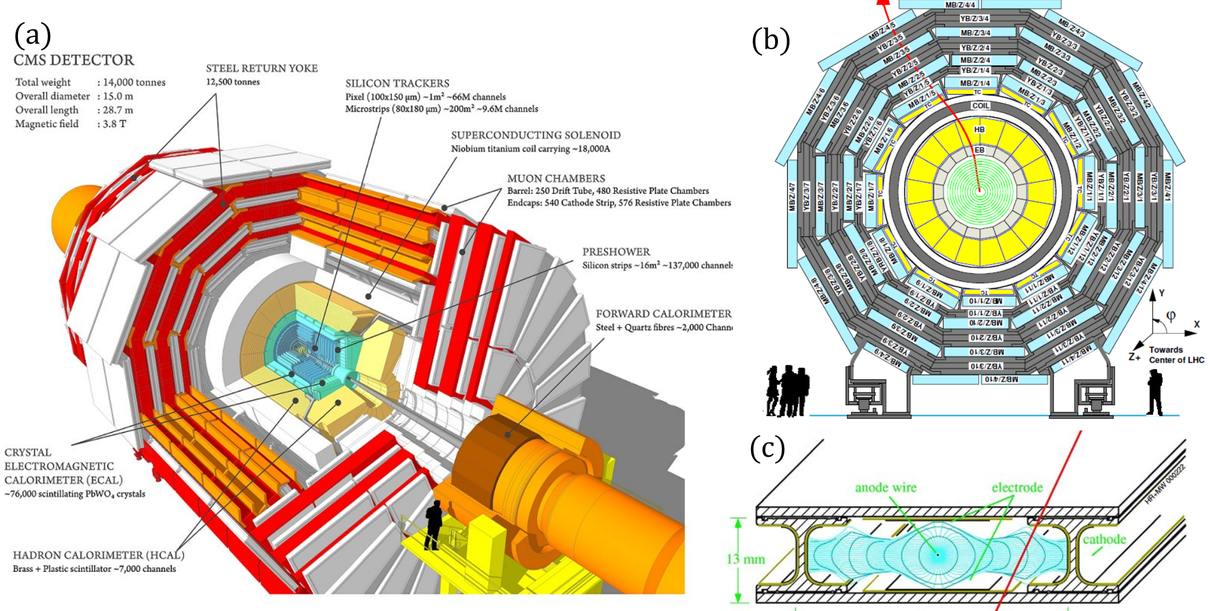
INTRODUCTION

The LHC is located at CERN in an underground tunnel 100 meters below the Franco-Swiss border. The machine is built with two beam pipes in a 26.7 km ring, consisting of superconducting magnets, which cross at four interaction points. Particles inside the machine are accelerated close to the speed of light and are made to collide at those four interaction points, in which four large experiment detectors are placed. CMS is located at point 5. The LHC machine will be upgraded at the end of run 3 and The High-Luminosity LHC will offer a fivefold increase in the machine's instantaneous luminosity. The CMS detector is being upgraded (Phase-2 Upgrade) in order to withstand the increased radiation, as well as the increased data rate from the products of the particle collisions.

CMS BARREL MUON SYSTEM

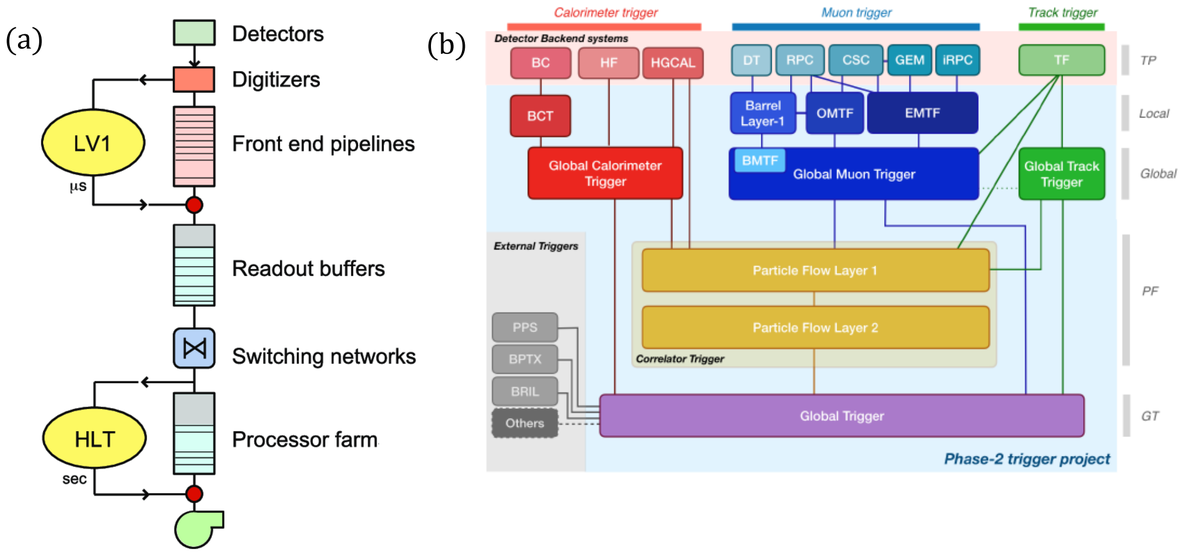
The barrel muon system consists of 2 types of gaseous detectors, Drift tube cells (DT) and Resistive Plate Chambers (RPC). The DT muon system is divided into five wheels, wheel -2, -1, 0, 1, 2 on the longitudinal view of the detector, while each wheel is divided into 12 Sectors on the transverse view. A muon hit is detected by passing through a DT cell and ionizing the gas.



(a) CMS detector (b) Transverse view of CMS with 12 sectors (C) Drift tube cell

TRIGGER SYSTEM

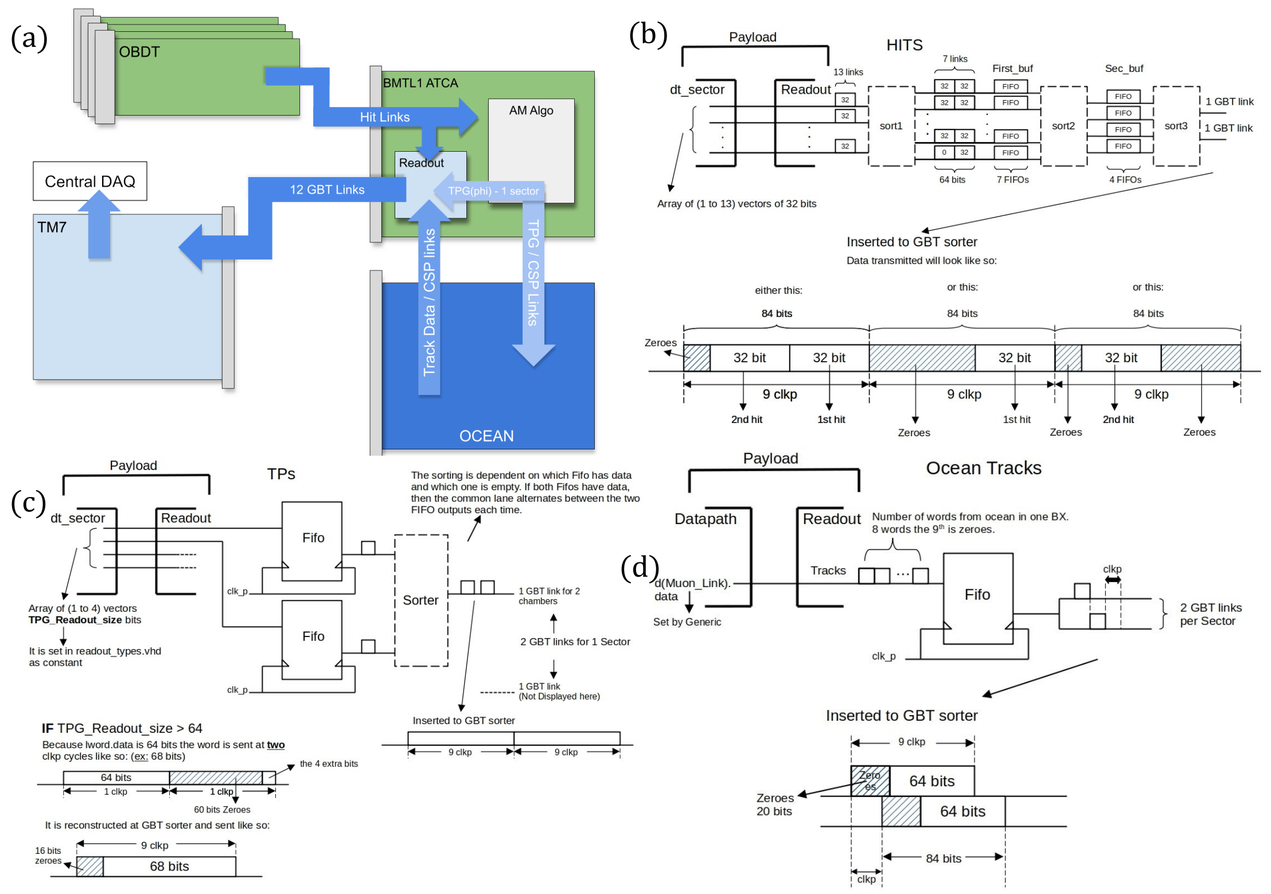
Proton-Proton Collisions at 40 MHz produce several tens of Petabytes of data every second. A Trigger system is in place in order to reduce the data rate. The Trigger system is divided in two stages. The Level-1 Trigger (L1T) uses custom made boards with FPGAs and high speed optical links in order to reduce the event rate to 750 KHz. Data stored in Readout buffers of the subsystems are transmitted to the Data Acquisition (DAQ) system upon arrival of the L1A signal which is ultimately created by the Global trigger physics menu. Data are then processed by the High Level Trigger (HLT) which uses commercial CPUs and GPUs, further reducing the event rate to 7.5 KHz. The data are then stored and subjected to further offline analysis.



(a) Trigger System (b) The Level-1 Trigger system with every subsystem from detector to Global Trigger

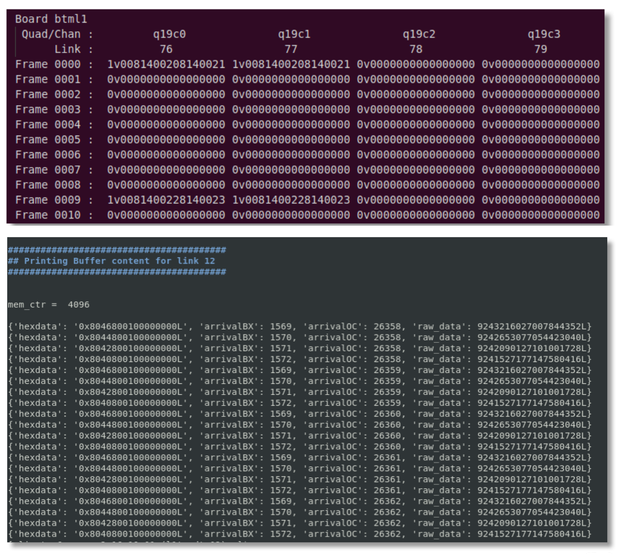
READOUT MODULE – USC SETUP

The Readout module written in VHDL as part of the firmware of the BMTL1 board, collects, stores and then transmits the data from three different sources. Hit data are delivered from the OBDTs installed at sectors 1 and sectors 12, containing the hits produced from ionization of DT cells. TPs (trigger primitives) are delivered from the Analytical Method algorithm running on the BMTL1 board which produces track segments based on the Hits. Muon tracks are delivered from the OCEAN board which performs the muon reconstruction of the barrel region with the Kalman Filter algorithm. The data are stored and then transmitted to a phase-1 TM7 board via 12 optical links with the GBT protocol, which in turn relays the data the Data Acquisition (DAC) system.



(a) Layout USC setup (b) Hit module (C) TP module (D) Track module

Data provided by the DT developer which contain Hit data were brought to the specified data format via a C++ program and were then injected into the system (BMTL1 firmware), this way simulating real Hit data delivered from the OBDTs. The created TPs and hits were then injected into the readout module as part of the normal dataflow. The readout module sorted them and transmitted them via the GBT protocol to the TM7 board. The data were then observed at the receiving end of the TM7 board via scripts and were found to be identical to the initially injected data at the BMTL1 board. The injection and capture of the data was performed with the IPbus protocol which allows the user to interface with a FPGA via the users' terminal.



(a) Data injected at the Readout Module (b) Data captured at the TM7 receiver buffers (c) BMTL1 board designed by University of Ioannina

CONCLUSIONS

The implementation of a Readout Design serves as a solution to monitor and evaluate data generated by the algorithms implemented on the Phase-2 boards while using Phase-1 boards until the system is complete. The Readout module offers a store and transmit mechanism, while using minimal FPGA resources. The addition of the module to the firmware does not add to the complexity of the framework, nor does it disrupt the normal behaviour of the rest of the system.

Ημερίδα του ΠΜΣ στις Σύγχρονες Ηλεκτρονικές Τεχνολογίες

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03 Ιουνίου 2024